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Class B Buffer Amplifier for LCD Display Driver System

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ABSTRACT: As with increasing number of pixels in the unit area of display panel means dpi of display, this will increase number of output buffer on the column driver chip for LCD display the static current and the die area should be minimum. This paper represents a small static loss buffer amplifier for large capacitive load of the flat panel, it support up to 1uF capacitive load at which the slew rate is 4V/µs , comparator are used in the buffer amplifier to turn on and off the push-pull output stage. The proposed buffer is implemented on 180 nm CMOS technology the output swing of the buffer is .8V-3.1V for the supply voltage 3.3V. The quiescent current of the proposed buffer is 20 µA and it is sufficient to drive the pixel of 1280 × 1024. With frequency of 50 kHz for the range of 256 gray levels.

I. INTRODUCTION

There are three requirements for the output buffer amplifier for LCD display first requirement is the number of output buffer which is increasing rapidly with the increasing terms of high resolution means the die area occupied by the buffer on the chip should be minimum, second requirement is the minimum power consumption as portability of electronic devices which are battery-operated increases the demand of low-power dissipation and the third requirement is the settling time of the buffer as output voltage must be settled within the horizontal scanning. Generally the horizontal scanning frequency ranges from 30-100 kHz. For a step size input the lower limit of output buffer is completed as 1/2f $C_L V_{DD} V_s$, f is signal frequency, C_L is the load capacitance, V_s is the voltage swing of column signal, & V_{DD} is the supply voltage. To reduce power dissipation, a class-A amplifier with variable bias current was used [3].

The amplitude of the output stage bias current is controlled by a digital pulse. In the first one-third of the scan-line period, a large bias current is used to make sure the output is settled within this period. For the rest of the scan-line period, a much smaller bias current is used to hold the output value. However, when the gray level does not change much in a column, this scheme wastes too much power. A dynamic biasing technique [4] was proposed to increase the bias current of the differential input stage of a two-stage amplifier, when the input voltage difference is large. This technique does not reduce the output-stage bias current. A class-B amplifier [5], [6] has a better power efficiency. But the sizes of the output transistors are large because the gate-to-source voltages are smaller than the supply voltage. To reduce both die area and power dissipation, another scheme [7] pre-charges the output to the supply voltage at the beginning of each scan-line period. Then the output voltage is discharged toward 0 V, and the output voltage is compared with the input voltage using a comparator. The discharging stops when the output voltage is equal to the input voltage. This scheme has no static power and is compact. However, it wastes dynamic power when the gray level in a column does not change much. Furthermore, its final voltage is always smaller than the input, due to the finite response time of the comparator.

II. PROPOSED CLASS B BUFFER AMPLIFIER

The schematic of proposed buffer is shown in figure 1 the buffer consists of the NMOS differential amplifier (M4,M5,M6 &M7), two comparators (M9,M10 & M11,M12) and push-pull output stage (M01 & M02). The comparators are used to sense the voltage difference applied at the input of differential pair, according to the input change the comparator turn on and off the push-pull output stage. The aspect of M10 & MM12 are chosen as, to ensure push-pull operation.

$$\left(\frac{W}{L}\right)_{10} = \frac{1}{2}\left(\frac{W}{L}\right)_6 + \Delta\left(\frac{W}{L}\right)$$

&

$$\left(\frac{W}{L}\right)_{12} = \frac{1}{2}\left(\frac{W}{L}\right)_6 - \Delta\left(\frac{W}{L}\right)$$

In stable mode when no input is applied to differential pair the output voltage is equal to input voltage, the current flowing in M4,M5,M7,M8,M9,M10,M11 & M12 are equal to I/2 where I is the biasing current. As the aspect ratio of M10 and M12 is made larger than half of the aspect ratio of M6 this will make M10 to come out from the situation and entered into triode region, this will make gate voltage of M02 to force towards Vss. M02 will stay at off condition, similarly the comparator M11 and M12 will made gate of M01 to force towards Vdd and make it off when no input is applied.

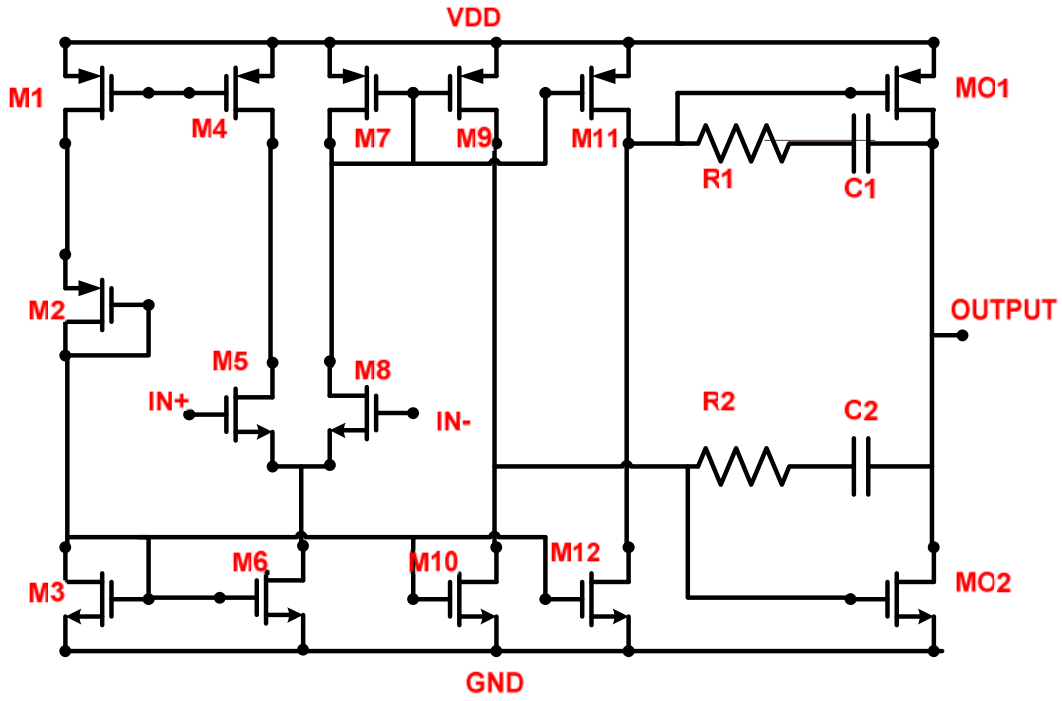

Fig. 1. Schematic of proposed buffer.

Now when there is ΔV voltage change is applied at non-inverting terminal the current in M5 is increased by an amount of $\frac{1}{2} g_m \Delta V_1$ with the same amount the current in M8 will decrease where g_m is the transconductance of M5 and M8. The current in M5 and M8 will be,

$$I_{D5} = \frac{I}{2} + \frac{1}{2} g_m \Delta V_1$$

$$I_{D8} = \frac{I}{2} - \frac{1}{2} g_m \Delta V_1$$

where

$$g_m = \sqrt{I\left(\frac{W}{L}\right)_5 \mu_n C_{ox}}$$

μ_n is the carrier mobility in the n-channel and C_{ox} gate oxide capacitance per unit area. The current in M7 is mirrored to M9,M11 and to the comparators also,i_{D8} is decreased by $\frac{1}{2}\, g_m \Delta V_1$ M10 will stay in triode region, and so M02 will be off, and if i_{D3} goes smaller than $\frac{I}{2}$- ΔI, which indicates that $\Delta V > 2\frac{\Delta I}{g_m}$

where $\Delta I = \frac{1}{2}\, I \left(\frac{W}{L}\right)_6 \mu_n C_{ox}(V_{GS6} - V_{th6})^2$

then the transistor M11 will be in saturation region this will decrease the gate voltage of M01 and M01 will turn on, this will charge the output node large of the value of ΔV more it will turn on M0 until it will turn on fully, now when the voltage difference between inverting input and output node will less than $2\frac{\Delta I}{g_m}$, then the gate voltage of M01 will start increasing, to start the charging of the output node, and a level is reached where M01 will turn off. Similarly when the input at noninverting terminal is reduced by ΔV from the stable state, M11 will stay at off, if ΔV is greater than $2\frac{\Delta I}{g_m}$ M10 will be in saturation and M02 gate voltage start to increase and this will discharge the output node until the voltage difference between input and output will be lower than $2\frac{\Delta I}{g_m}$ then M02 gate voltage start increasing and it will turn off the M02. The whole process is summarized as:

1. When $V_{in}^- - V_{out} > 2\frac{\Delta I}{g_m}$ M01 will charge the output node.
2. When $V_{in}^- - V_{out} \leq 2\frac{\Delta I}{g_m}$ M01 will discharge the output node.
3. When $-2\frac{\Delta I}{g_m} \leq V_{in}^- - V_{out} \leq 2\frac{\Delta I}{g_m}$ then both M01 and M02 will be off.

III. POWER CALCULATION

Power dissipation in any electronic circuit is composed of static power consumption and dynamic power consumption is static power consumption is due to biasing current flowing under no input condition and dynamic power consumption is due to charging and discharging of output node.

For any circuit the static power consumption at particular frequency (scanning frequency) is expressed as:

$$E_{static} = \frac{I_{bias} V_{DD}}{f_{scanning}}$$

I_{bias} is the biasing current in the electronic network, $f_{scanning}$ is the scanning frequency during which the circuit is on, V_{DD} supply voltage.

The dynamic power consumption is depend upon,

1. Charging of the output node,

$$P_{charge} = (V_{DD} - V_0) i_L = (V_{DD} - V_0) C_L \frac{dV_o}{dt}$$

So energy dissipated will be

$$E_{charge} = \int_{V_L}^{V_H} P_{charge}\, dt$$

$$= (V_H - V_L) C_L V_{DD} - \frac{1}{2} C_L (V_H^2 - V_L^2)$$

2. Discharging of output node,

$$P_{discharge} = -V_0 i_L = -V_0 C_L \frac{dV_o}{dt}$$

So energy dissipated during discharging will be

$$E_{charge} = \int_{V_L}^{V_H} P_{charge}\, dt = \frac{1}{2} C_L (V_H^2 - V_L^2)$$

Now total energy dissipated by the buffer amplifier during charging and discharging for one period of scanning frequency will be

$$E_{tot,charge+discharge} = \frac{I_{bias} V_{DD}}{f_{scanning}} + (V_H - V_L) C_L V_{DD} - \frac{1}{2} C_L (V_H^2 - V_L^2)$$

$$+ \frac{I_{bias} V_{DD}}{f_{scanning}} + \frac{1}{2} C_L (V_H^2 - V_L^2)$$

So the total average power dissipated by a buffer amplifier for one scanning period will be, $P_{total} = f_{scanning} E_{total}$

IV. EXPERIMENTAL RESULT

The proposed buffer was implemented on UMC 180nm CMOS technology, the dynamic power consumption will be maximum when the pixel will alternate with black-and-white contrast the power dissipation was calculated by the above equation under the different scanning frequency. In figure 2 shows dynamic power consumption of the proposed buffer under one microphone and capacitive load the average dynamic power consumption was around 3m watt, and the static power consumption is around 198 µW. Figure 3 shows current change during dynamic change in input for the trail transistors M3,M6,M10 and M12. Figure 4 shows the output step response of the proposed buffer with 50 kHz square wave under the load condition of 1 µf capacitance. Figure 5 shows triangular response of the proposed buffer for 50 kHz triangular wave under the load condition of 1 µf. Figure 6 shows frequency response of the proposed buffer for the load capacitance of 1 µf.

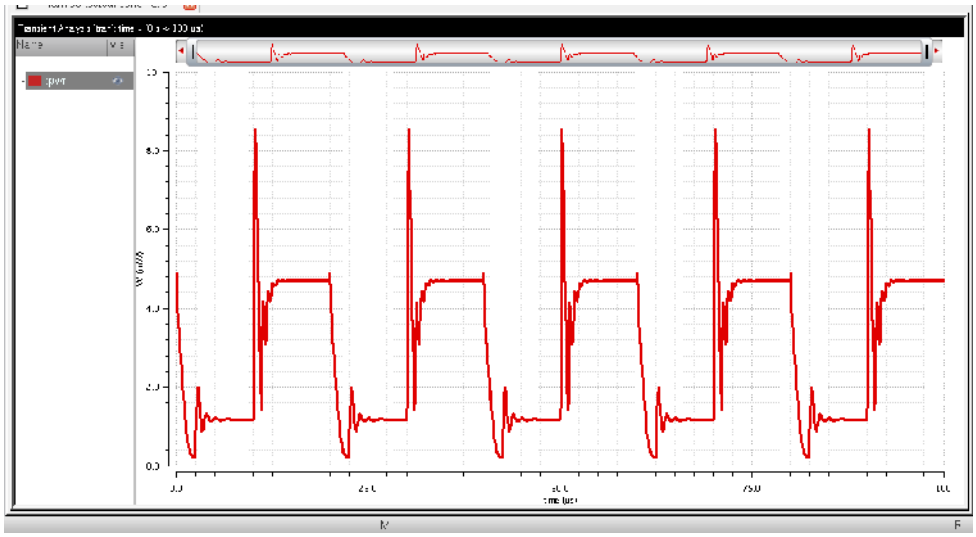

Fig. 2. Dynamic power dissipation by the proposed buffer.

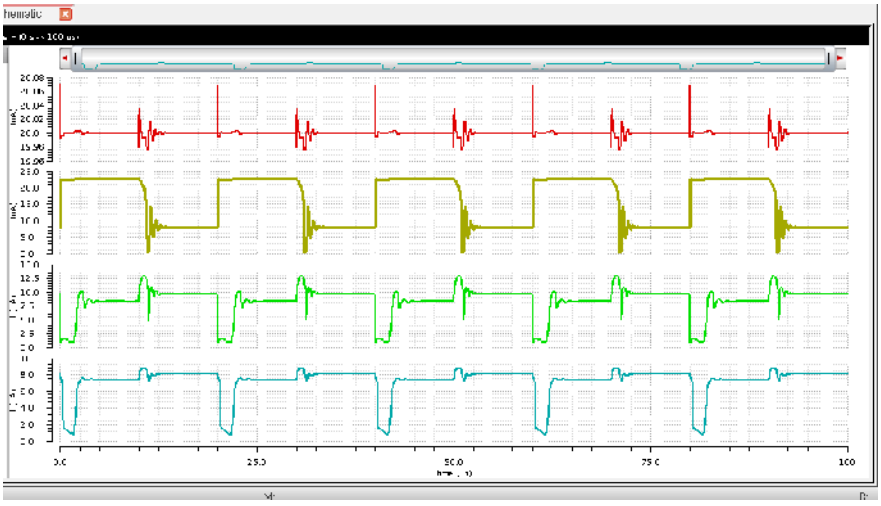

Fig. 3. Drain current at the transistors M3,M6,M10 and M12.

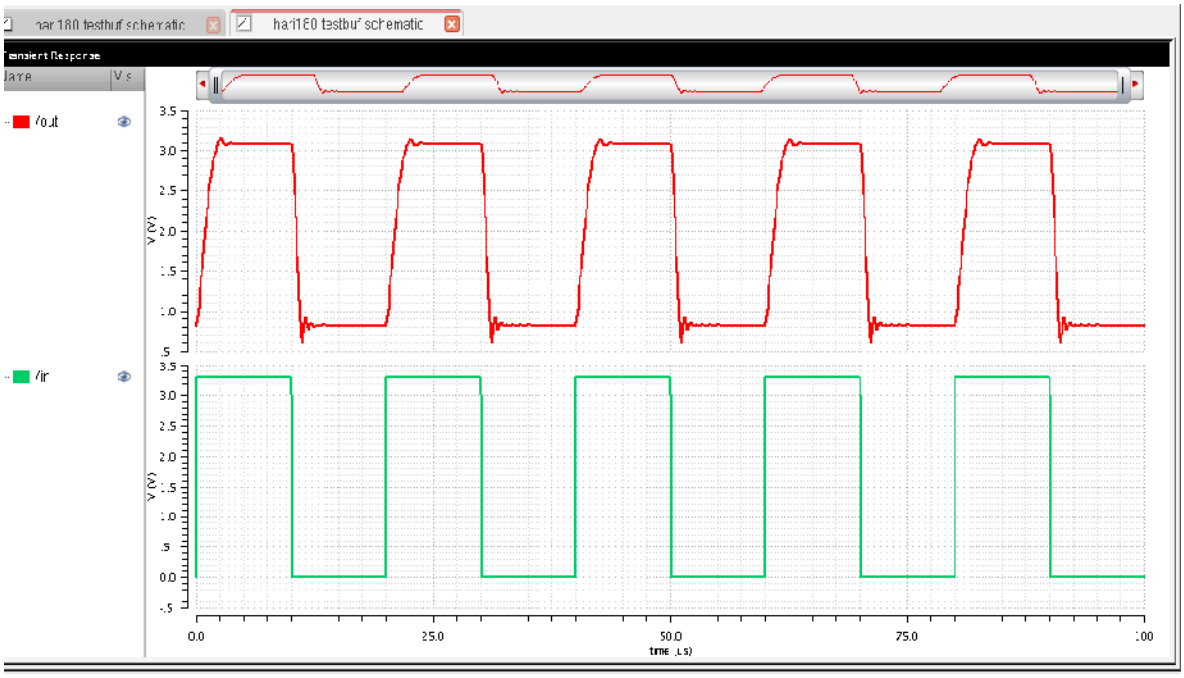

Fig. 4. Step response of the proposed buffer with 50 kHz square wave for 1µf capacitive load.

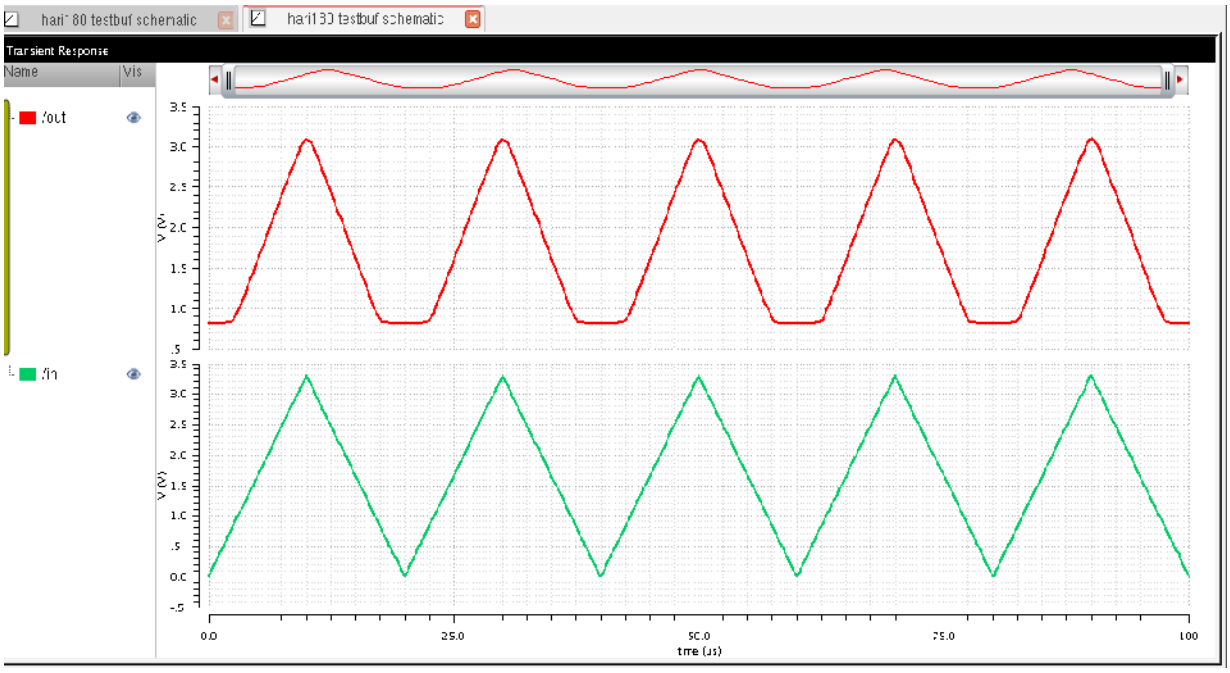

Fig. 5. Triangular response of the proposed buffer with 50 kHz triangular wave for 1µf capacitive load.

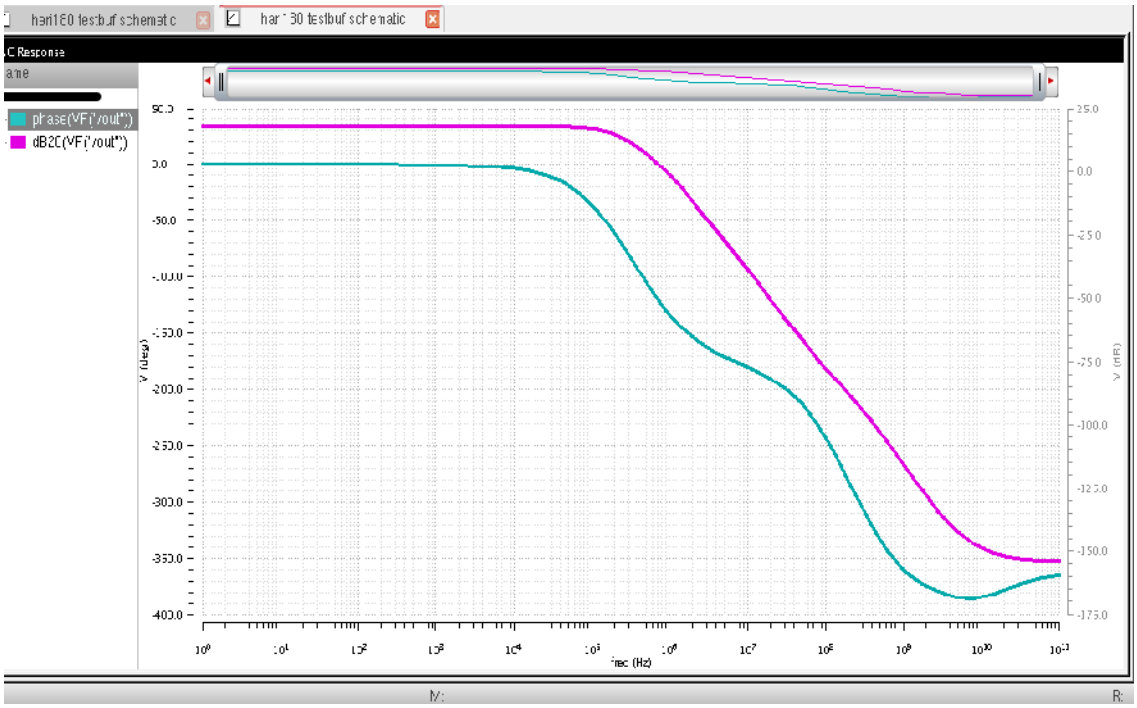

Fig. 6. AC response of the proposed buffer amplifier.

V. CONCLUSION

In this paper we demonstrate in low-power consumption high-speed class B buffer amplifier which is suitable for flat panel display application for large capacitive column lines of the panel the driving capability of the circuit was enhanced by using two comparators with senses rising and falling edges of the input way and according to which turned on and off the push-pull output stage, push pull output is stage will be off when no input is applied this will save static power loss, the step response for 0-3.3V input swing the output swing will be .8V - 3.1 V for 1µf capacitive load. The biasing current of the proposed buffer amplifier is 20 µA, the rising and falling one-time is around 1.6 and 1.4 µs for the1µf capacitive load.

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